REMARKS

Claims 3-10 and 13-24 were pending in this application. Claims 3-10 and 13-24 will remain after this amendment.

Claim 3 has been amended to clarify "an attachment bus coupled to the host processor, the attachment bus being inside the computer system" and the "peripheral device," which is "coupled to the host processor via an attachment bus."

The Office Action rejected Claims 3-5, 7-10, 13-20, 22-23 under 35 USC 102(e) as being anticipated by Marin (6,088,734). Marin teaches a "network" of "ATM nodes," and "communication between the nodes" (Fig. 2 and col. 6, lines 25-30). The Office Action cited columns 6-7 of Marin, which relate to a "node" evaluating "whether the cost of service parameters of the request [to access the ATM network] may be met by a route through the ATM network before the connection request is accepted."

In contrast, Applicant's independent Claims 3, 6 and 9 each recite a "computer system" with a "peripheral device" that transfers data "from a network" to a "host processor" over an "attachment bus inside the computer system." Claims 13 and 18 recite methods of "transferring data from a network to a host processor over an attachment bus inside the computer system." Claims 23 and 24 each recite a "peripheral device coupled between a host device and a network, the peripheral device operable to transfer data packets from the network to the host device over an attachment bus inside the computer system." Marin describes operations for nodes on a network, not "computer systems," "peripheral devices" and methods for transferring data from a network to a host processor over an attachment bus inside the computer system, as recited in Claims 3, 6 and 9. A cited

patent should disclose each and every element of a claim to be considered 35 USC 102 prior art. Marin does not disclose or teach each and every element of independent Claims 3, 6, 9, 13, 18, 23 and 24.

The Office Action stated Marin teaches the "host processor" of Claim 3. Marin briefly states "computer program instructions" may be executed by a "processor" in col. 6, lines 7-10. But Marin does not show or describe a "host processor" coupled to a "peripheral device" via an "attachment bus" and receiving data from the "peripheral device," as recited in Claim 3.

The Office Action stated Marin teaches the "peripheral device" of Claim 3. Marin does not teach "a peripheral device configured to transfer data from a network to the host processor over an attachment bus inside the computer system using at least first and second types of data transfers," as recited in Claim 3. The "first and second types of data transfers" are explained in the last paragraph of Claim 3, which recites the "peripheral device" has a "control circuit" "configured to place at least a minimum amount of data from the first queue onto the attachment bus during each time cycle; where the control circuit is configured to place data from the second queue onto the attachment bus only when the attachment bus is otherwise unoccupied by first class data." Marin does not disclose transferring data from a "peripheral device" to a "host processor over an attachment bus inside the computer system using at least first and second types of data transfers," as recited in Claim 3.

In addition, Marin does not teach "a control circuit configured to place data from the first queue onto the attachment bus at a higher priority than data from the second

queue is placed onto the attachment bus," as recited in Claim 3. Cols. 7 and 10-12 of Marin only teach placing data in "input queues 52a, 52b" and a "main queue 54." Marin does not teach placing data "from the first queue onto the attachment bus at a higher priority than data from the second queue is placed onto the attachment bus," as recited in Claim 3.

The Office Action cited col. 10, lines 11-35 of Marin as disclosing a "bus" of Claim 3 "configured to receive data during time cycles of predetermined length." Col. 10, lines 11-35 of Marin describe "cells" with "timestamps." Each timestamp "is preferably the sum of the arrival time of the cell at the scheduler 50 and the delay guarantee associated with the connection to which the cell belongs." These lines in Marin do not teach a "bus" "configured to receive data during time cycles of predetermined length," as recited in Claim 3. Marin as a whole does not even mention the word "bus."

For the reasons stated above, amended Claim 3 and dependent Claims 4, 5, 7 and 21-22 should be allowable over Marin.

Claim 9 should be allowable over Marin for the reasons stated above for Claim 3.

The Office Action cites col. 6, lines 25-44 of Marin as teaching a "classifying circuit" that "includes a storage device that stores information indicating each of the virtual channels that is associated with at least one of the classes," as recited in original Claim 9. Claim 9 has been amended to clarify the "storage device," which "stores a list of virtual channel identifiers that are associated with at least one of the classes." This amendment is supported by pages 7-8 of the specification and Fig. 2. Marin does not teach a "storage device that stores a list of virtual channel identifiers that

are associated with at least one of the classes," as recited in amended Claim 9.

Dependent Claim 10 should be allowable over Marin because Marin does not teach a "selection element" that compares the "virtual circuit identifier in the packet to the virtual channel identifiers stored in the storage element," as recited in Claim 10.

The Office Action rejected Claims 13-17 for the same reasons as Claims 3-5 and 7-8. Claims 13-17 should be allowable over Marin for the reasons stated above.

The Office Action rejected Claims 18-19 for the same reasons as Claims 9 and 10. Claims 18-19 should be allowable over Marin for the reasons stated above.

The Office Action cited col. 7, lines 26-52 of Marin as teaching Claim 20. Marin does not teach "a shift register adapted to store a portion of the received packet, and the storage device is a content addressable memory (CAM) device adapted to store virtual channel identifiers that are associated with at least one of the classes," as recited in amended Claim 20. Marin does not disclose any specific types of memory. Claim 20 should be allowable over Marin.

The Office Action rejected Claim 23 for the same reasons as Claim 3. Claim 23 should be allowable over Marin for the reasons stated above. As stated above, Marin does not disclose or teach a "peripheral device coupled between a host device and a network," as recited in Claim 23.

The Office Action rejected Claims 6, 21 and 24 over Marin in view of Gulick (6,470,410). As stated above, Marin does not teach a "peripheral device" transferring data from a network to a "host processor" or "host device" over a bus, as recited in Claims 6, 21 and 24.

In addition, Marin does not teach that a "first type of transfer associated with the first class of data is an isochronous transfer, and the second type of transfer associated with the second class of data is a bulk transfer," as recited in Claim 6. The Office Action cited col. 10, lines 21-54 of Marin, but these lines do not teach the "isochronous" and "bulk" transfers recited in Claim 6.

Gulick also fails to teach the "isochronous" and "bulk" transfers of Claim 6.

The Office Action cited Gulick as teaching a USB in a computer system, as in Claim 6. Gulick teaches a "USB host controller 1912" in col. 24, line 45. But Gulick does not teach the "peripheral device," "host processor," "bus," "control circuit," "isochronous transfer," and "bulk transfer," as recited in Claim 6, which Marin fails to teach.

Claim 6 has been amended to clarify the recited computer system with "a peripheral device configured to receive asynchronous transfer mode (ATM) data packets from a network and transfer data to the host processor over an attachment bus inside the computer system."

The combination of Marin and Gulick does not teach a "peripheral device" that receives "asynchronous transfer mode (ATM)" packets from a network, separates the data into first and second classes, and transfers the data to a "host processor" over a "Universal Serial Bus (USB)" using "isochronous" and "bulk" transfers, as recited in amended Claim 6.

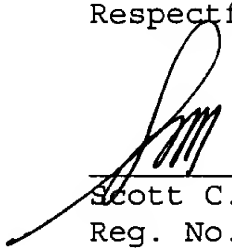
The Office Action cited Gulick as teaching a PCI bus, as in Claim 21. Claim 21 depends on Claim 3. Gulick does not teach all the limitations of Claim 3 that Marin fails to teach, which are described above.

The Office Action rejected Claim 24 for the same reasons as Claim 6. Claim 24 should be allowable over Marin for the reasons stated above.

Applicant respectfully requests that all pending claims be allowed. No fees are believed to be due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: January 9, 2004



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